Technology Leadership Day 2003

FPGA Developments and Trends:

Example of a DSP for Medical Applications

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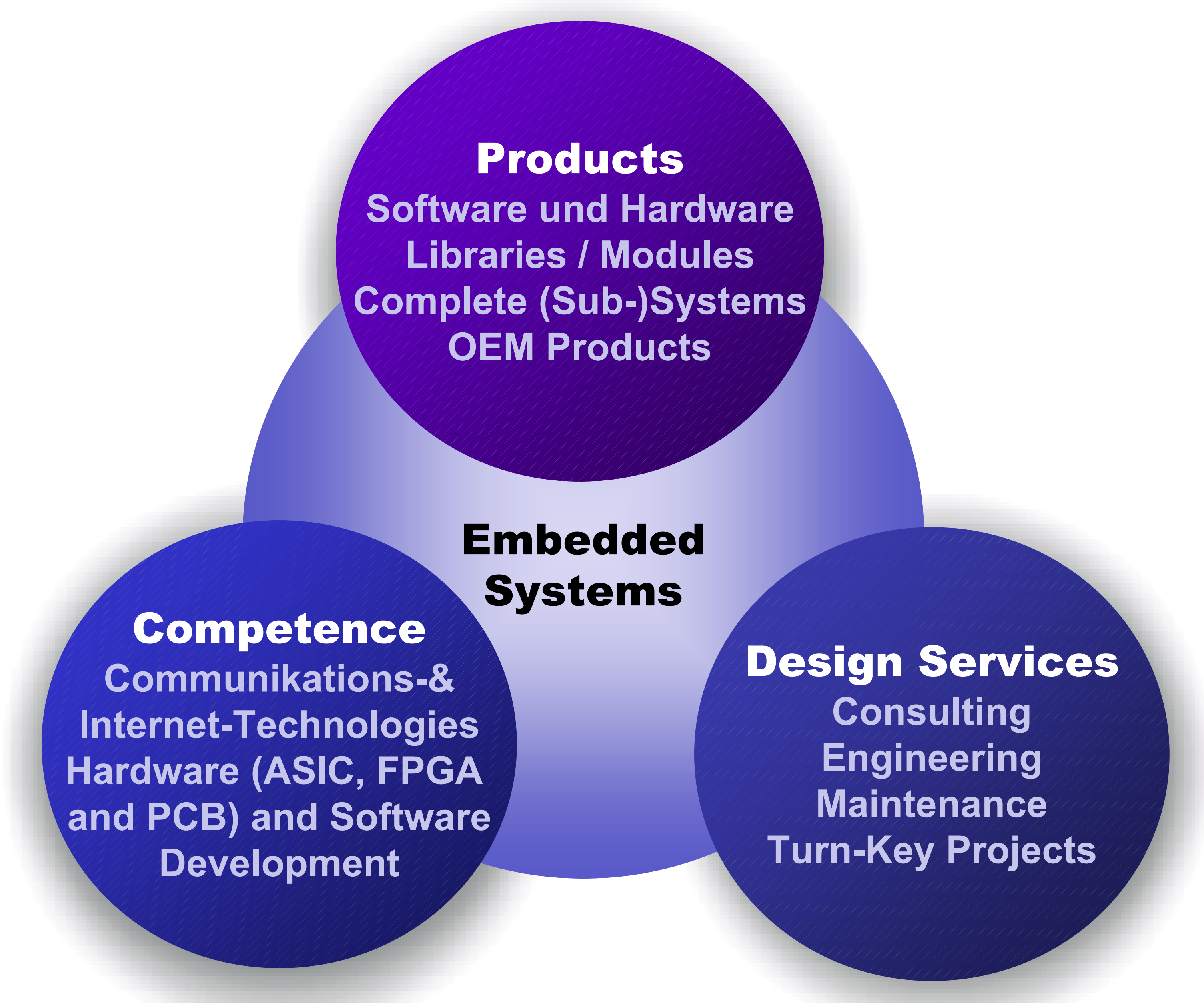
1.9.03: The Hardware Design Team of INITEC AG joined Netmodule AG



Overview

Part 1: Trends in high-end FPGA's

- Complexity up to 8 Million "System Gates"
- Embedded processors (RISC, Power PC, DSP)
- Embedded "Clock Managers" for clock skew control and clock synthesis
- Wide range of I/O standards. Includes high speed, low voltage and differential signaling

Part 2: Example of a DSP for a medical application

- System Clock of 120MHz
- Microcoded Sequencer for complex scanning patterns
- Interchip communication by means of LVDS double data rate links (>2500Mbit/s per link)
- 512kbit on-chip memory for signal delay

Complexity

- **Example: Virtex II (Xilinx)**

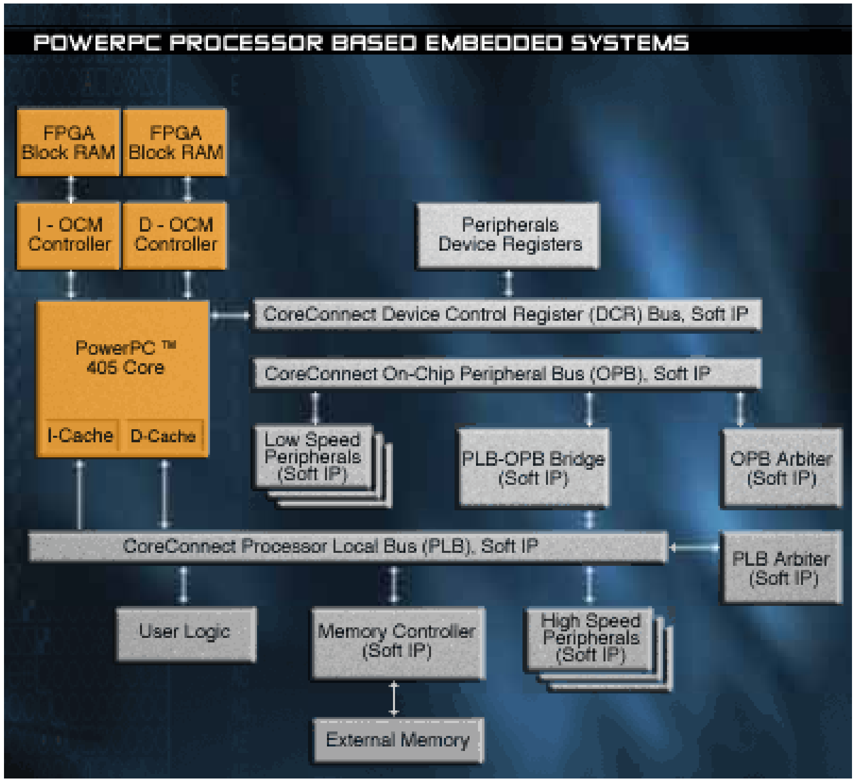
Device	System Gates	Registers	RAM
XC2V40	40k	512	72kbit
XC2V1000	1M	10‘240	720kbit
XC2V8000	8M	93‘184	3‘024kbit

up to 12 DCM
up to 1‘108 I/O pads

Embedded Processors

Hard Cores

- **Xilinx Virtex II PRO:**
  1-4 IBM PowerPC 405 cores



Soft Cores

- **Altera: Nios**
  16 or 32bit RISC CPU
  f_{max} over 125MHz
  library of standard configurable peripherals
  plug for custom instructions
  CPU uses 1000.. 1500 logic elements

- **Xilinx: Microblaze**
  32bit RISC CPU
  fmax = 125MHz
  large choice of IP for peripherals

Digital Clock Manager

- **Clock De-skew:**
  The DCM generates new system clocks (either internally or externally to the FPGA), which are phased-aligned to the input clocks.
  This eliminates clock distribution delays.
  Example: Required for interfacing high speed ZBT RAM

- **Frequency Synthesis:**
  The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.

- **Phase Shifting:**
  The DCM provides both coarse and fine-grain phase shifting with dynamic phase control.

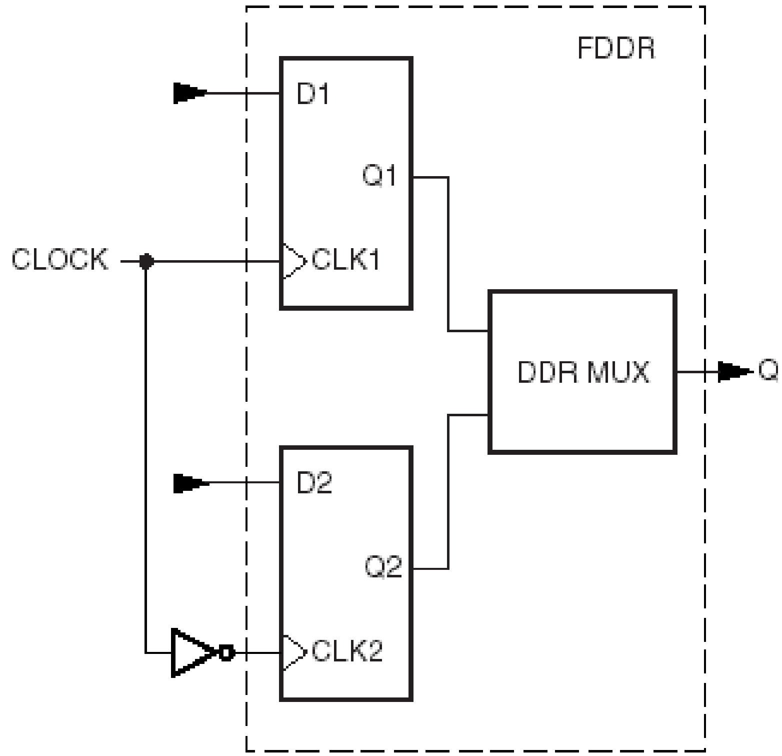
Versatile Input/Output Circuits

Wide Range of IO Types

- LVTTL
- LVCMOS
- PCI
- GTL
- HSTL
- SSTL

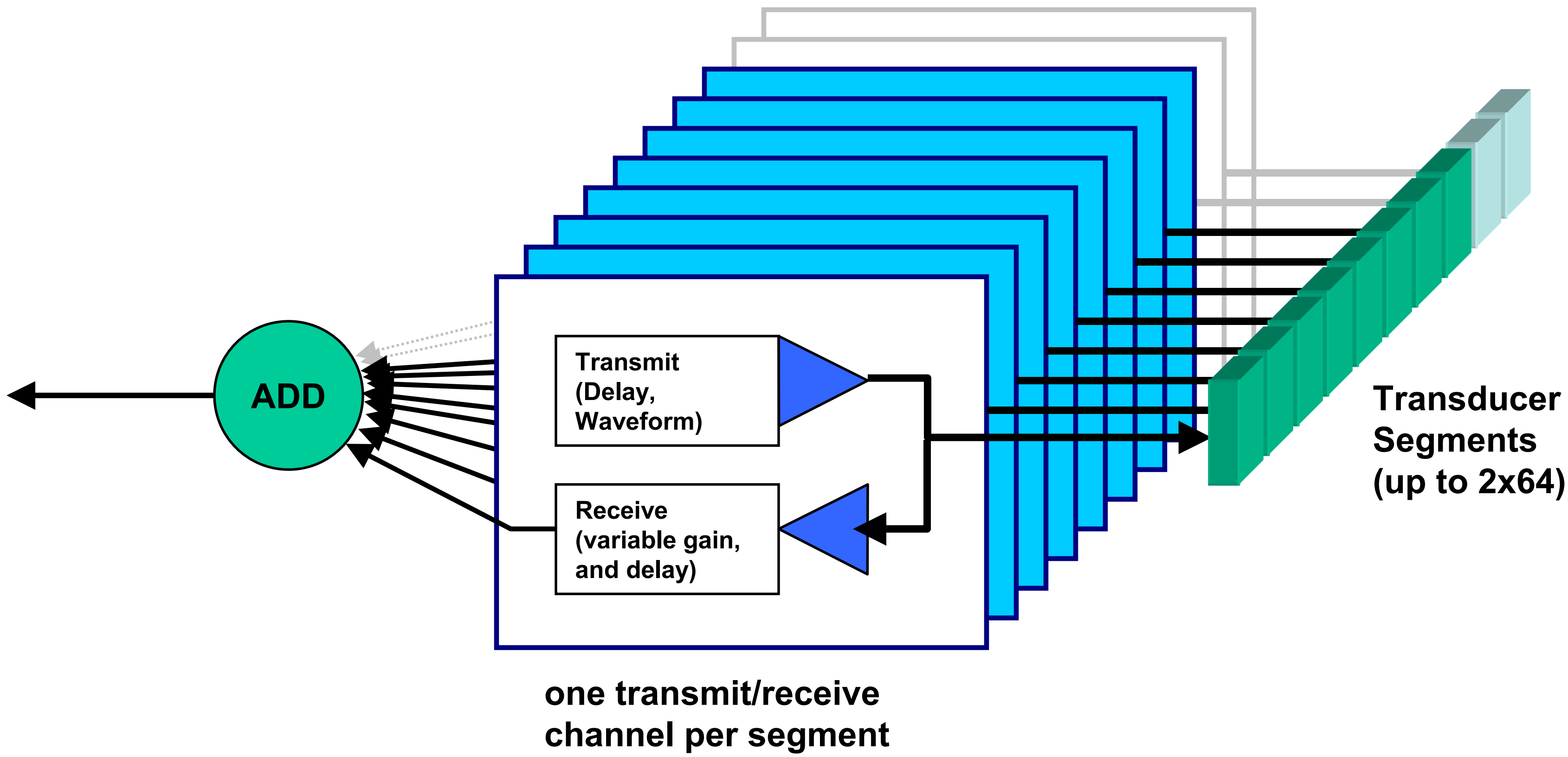
- LVPECL
- LVDS

Double Data Rate IO



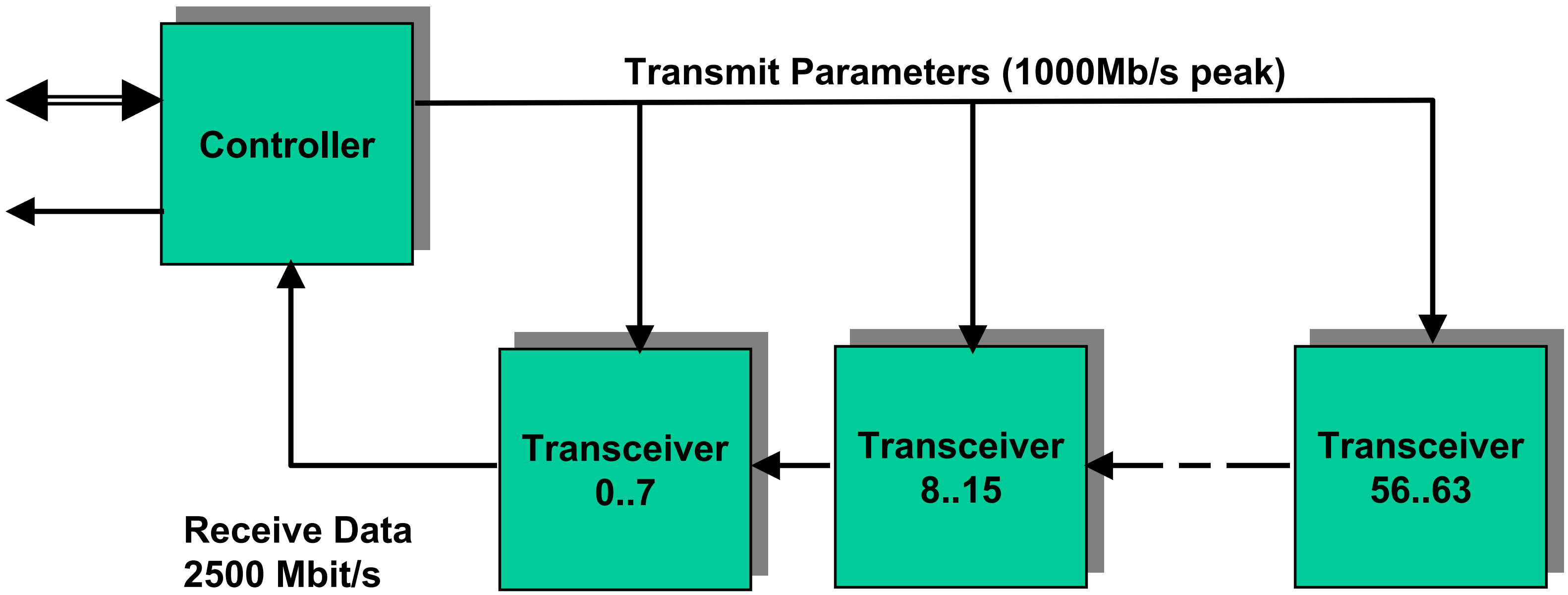
Digital Beamformer for Medical Ultrasound

- **64 parallel transmit-receive channels**
- **For each channel delay control (6ns resolution)**

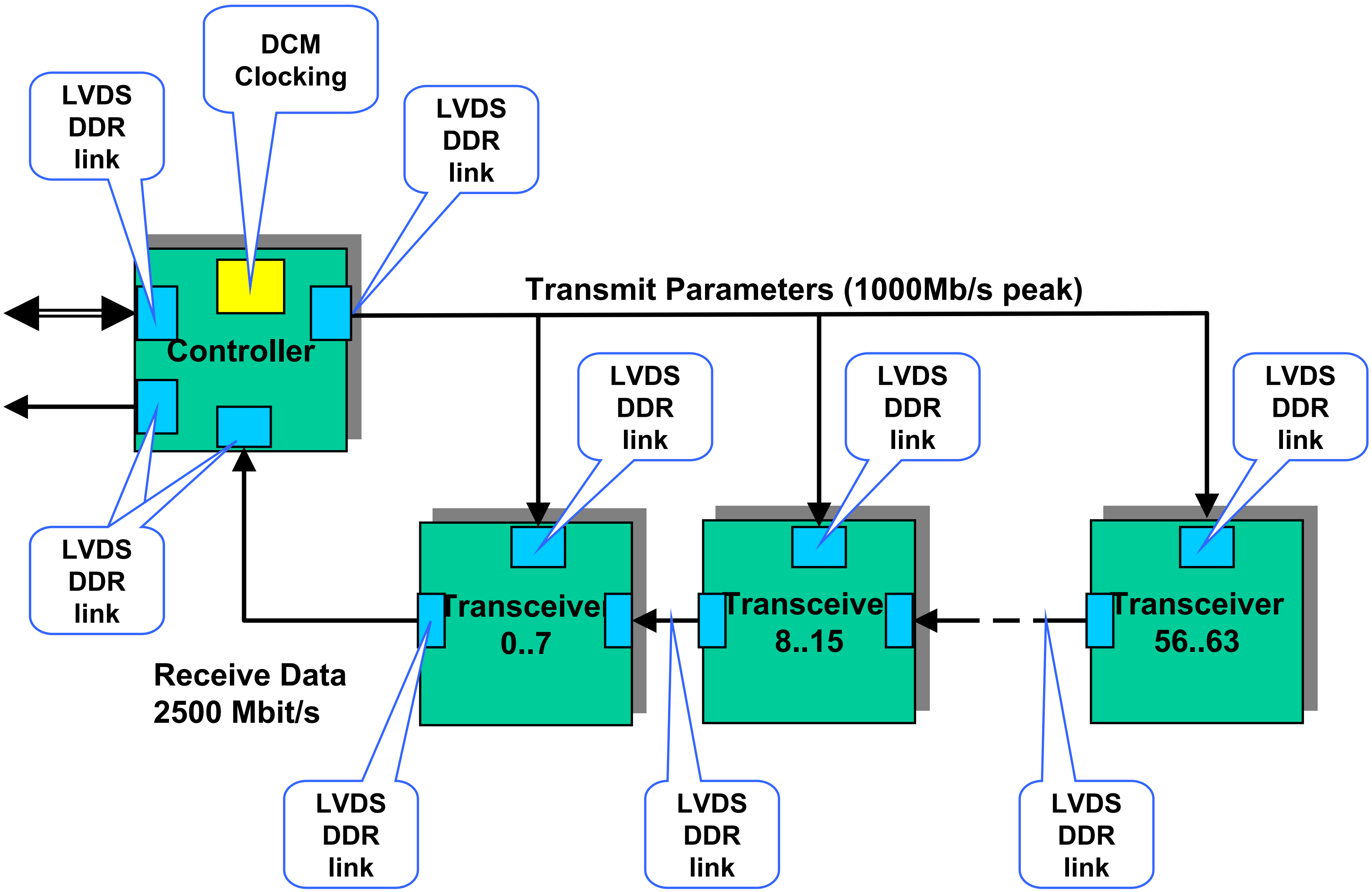


Digital Beamformer for Medical Ultrasound (2)

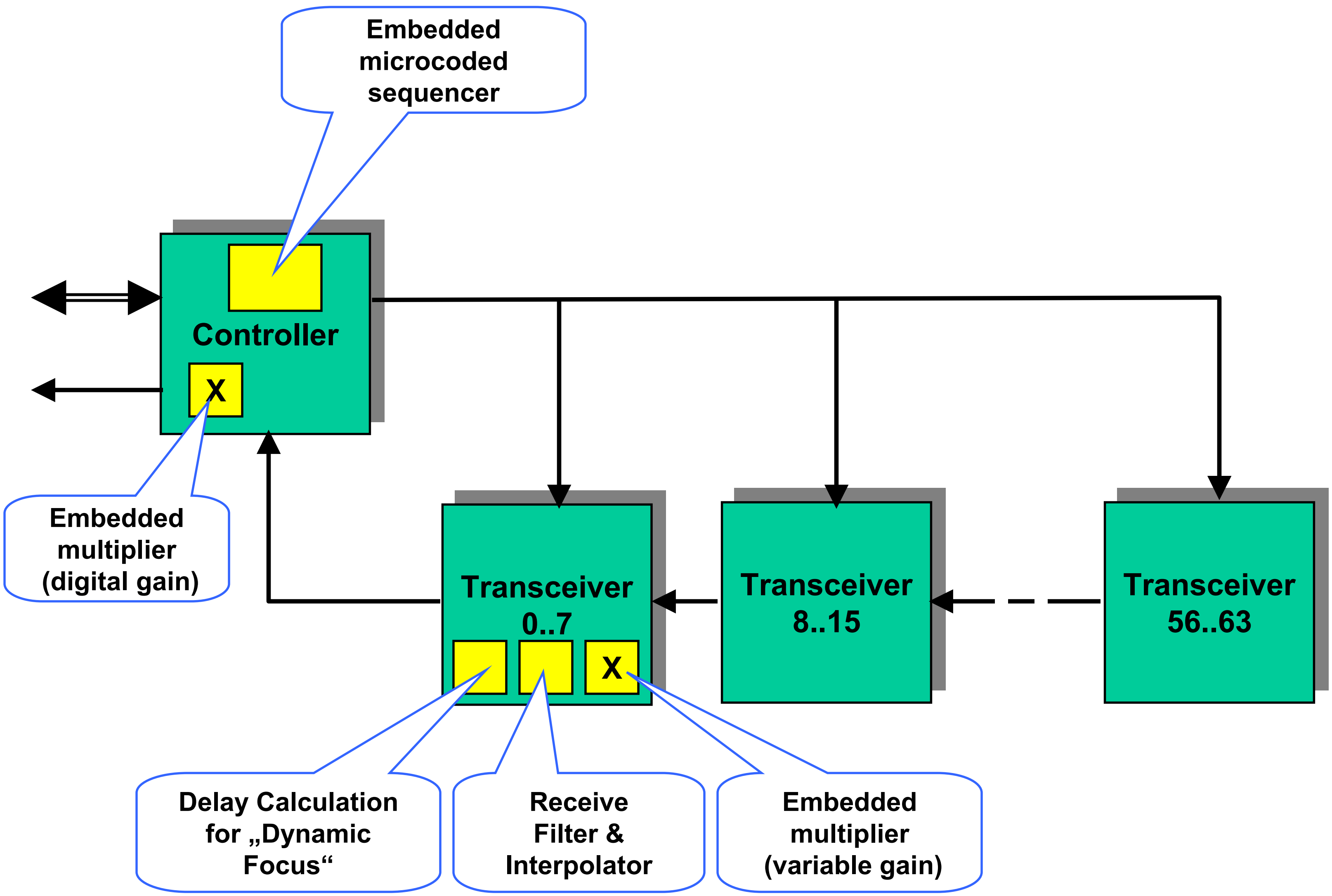
- **Complete Beam Former**
  = Controller + 8 octal Transceivers



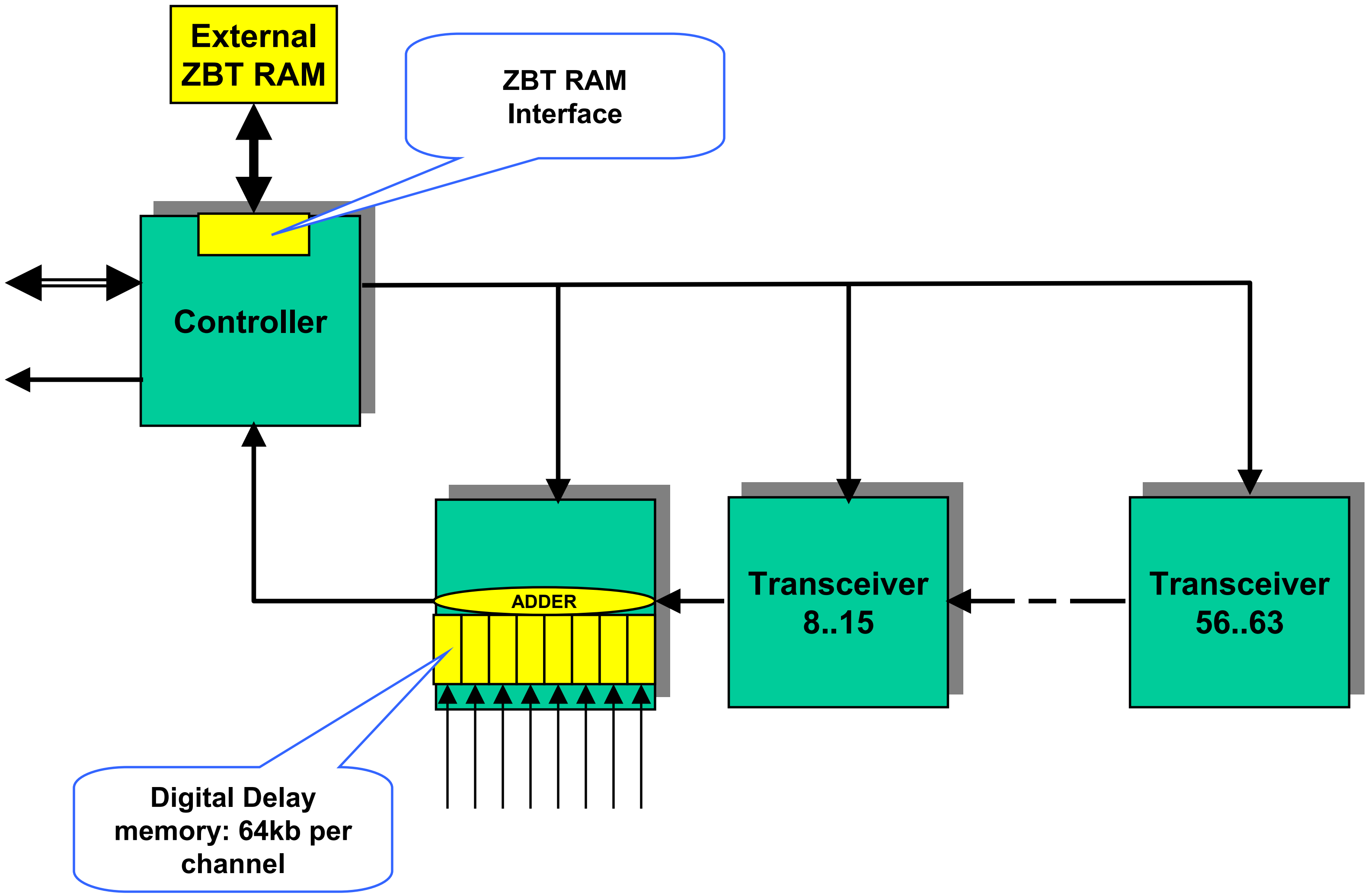
Using the FPGA‘s Key Features (links and clocks)



Using the FPGA‘s Key Features (processors)



Using the FPGA's Key Features (memories)



Design Flow (1)

- **Requirements Specification:**
  Word document organized according to „Structured Analysis and Design“ Methodology

- **Implementation:**
  VHDL ´93 on Visual VHDL (Summit Design Inc.)

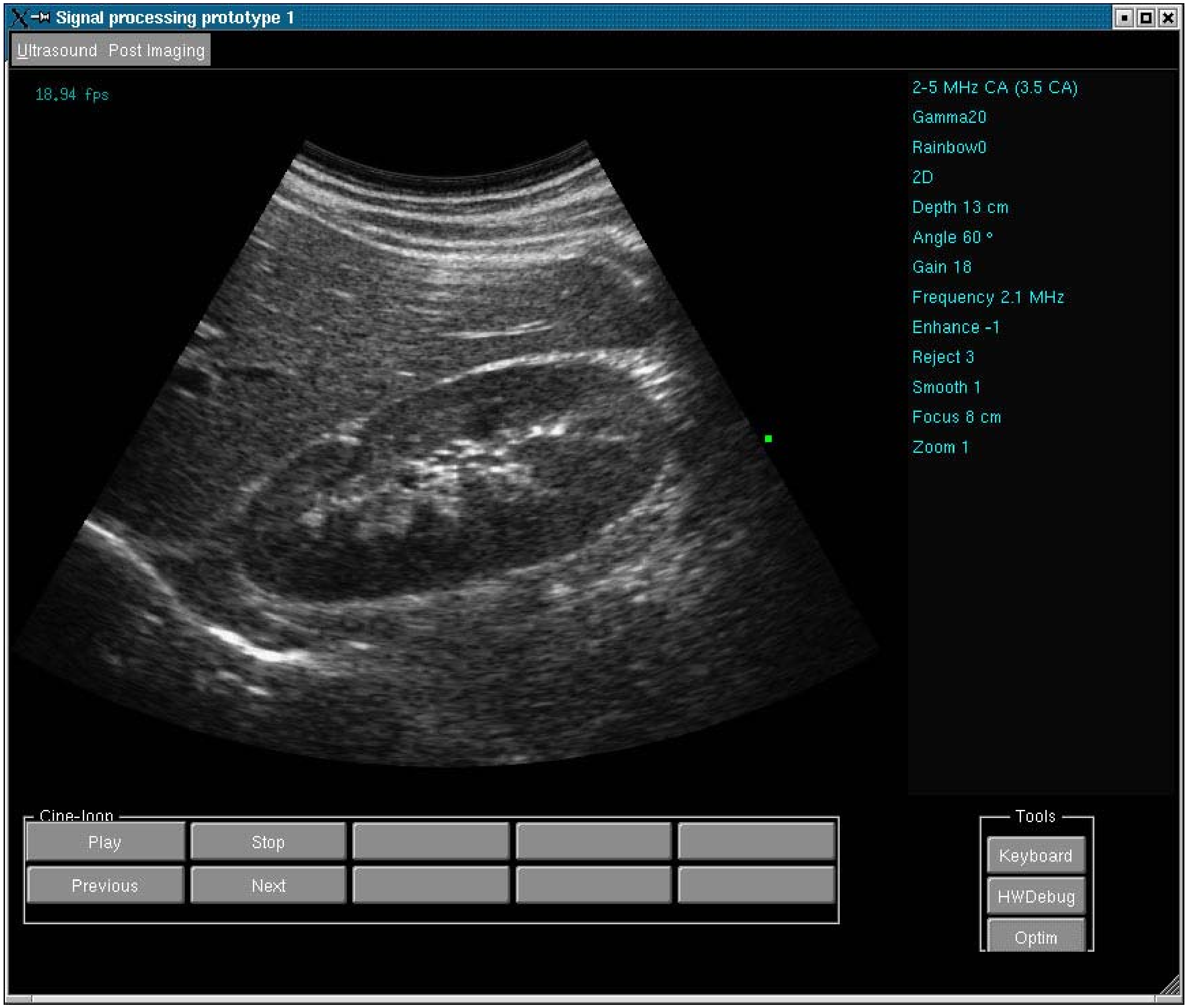
- **Verification:**
  RTL Level Testbenches (Visual HDL)
  - Testbench contains a dedicated parser
  - Stimulus written using scripting language (ASCII file)
  - Testbench output is ASCII logfile
  - Partially selfchecking for easy regression testing

Design Flow (2)

- **Synthesis:**
  Synplify with HDL Analyst (Synplicity Inc.)

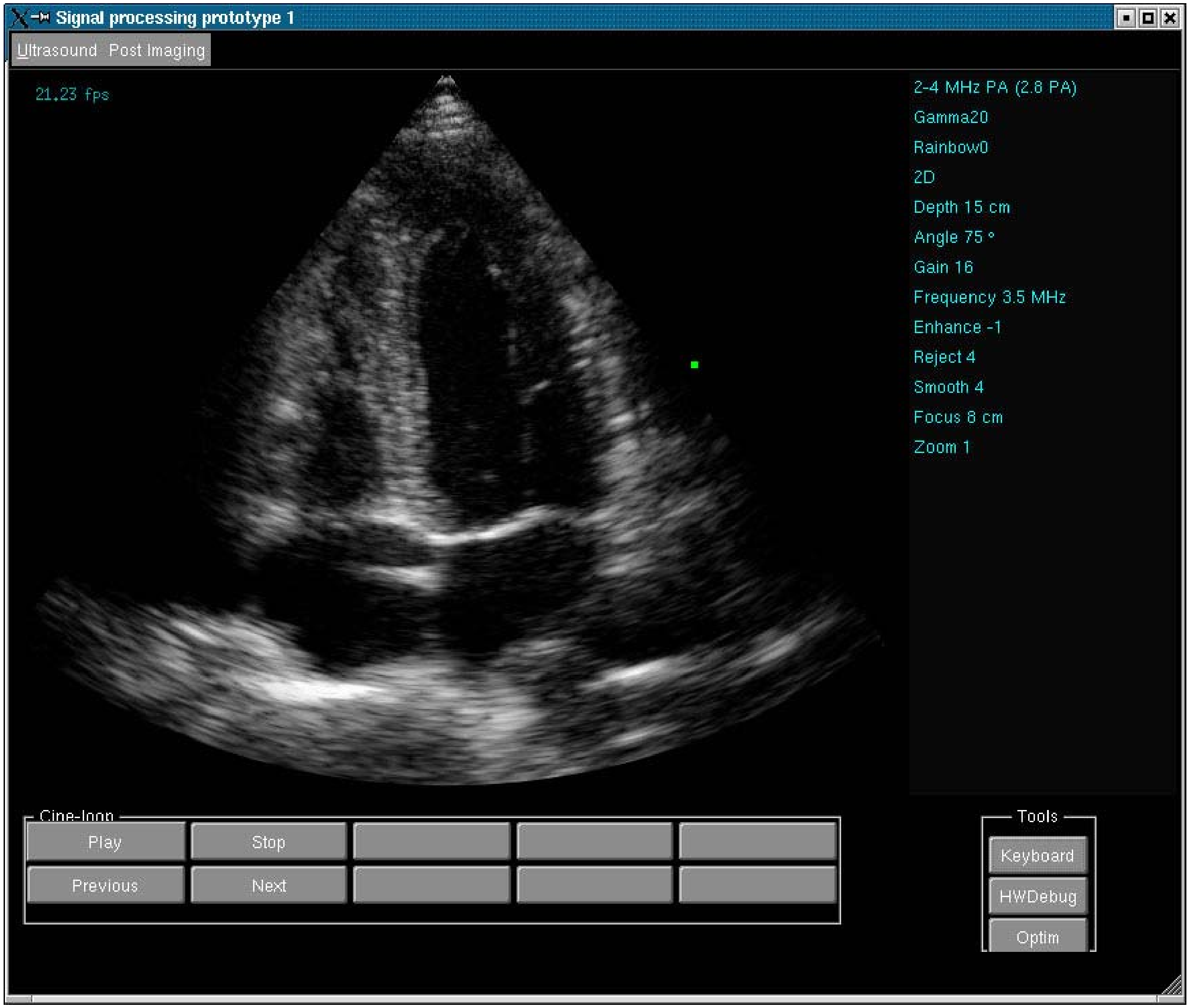
- **Place-and-Route:**
  Xilinx Foundation
  - guided placement of clock elements and critical interface modules

Results: Kidney



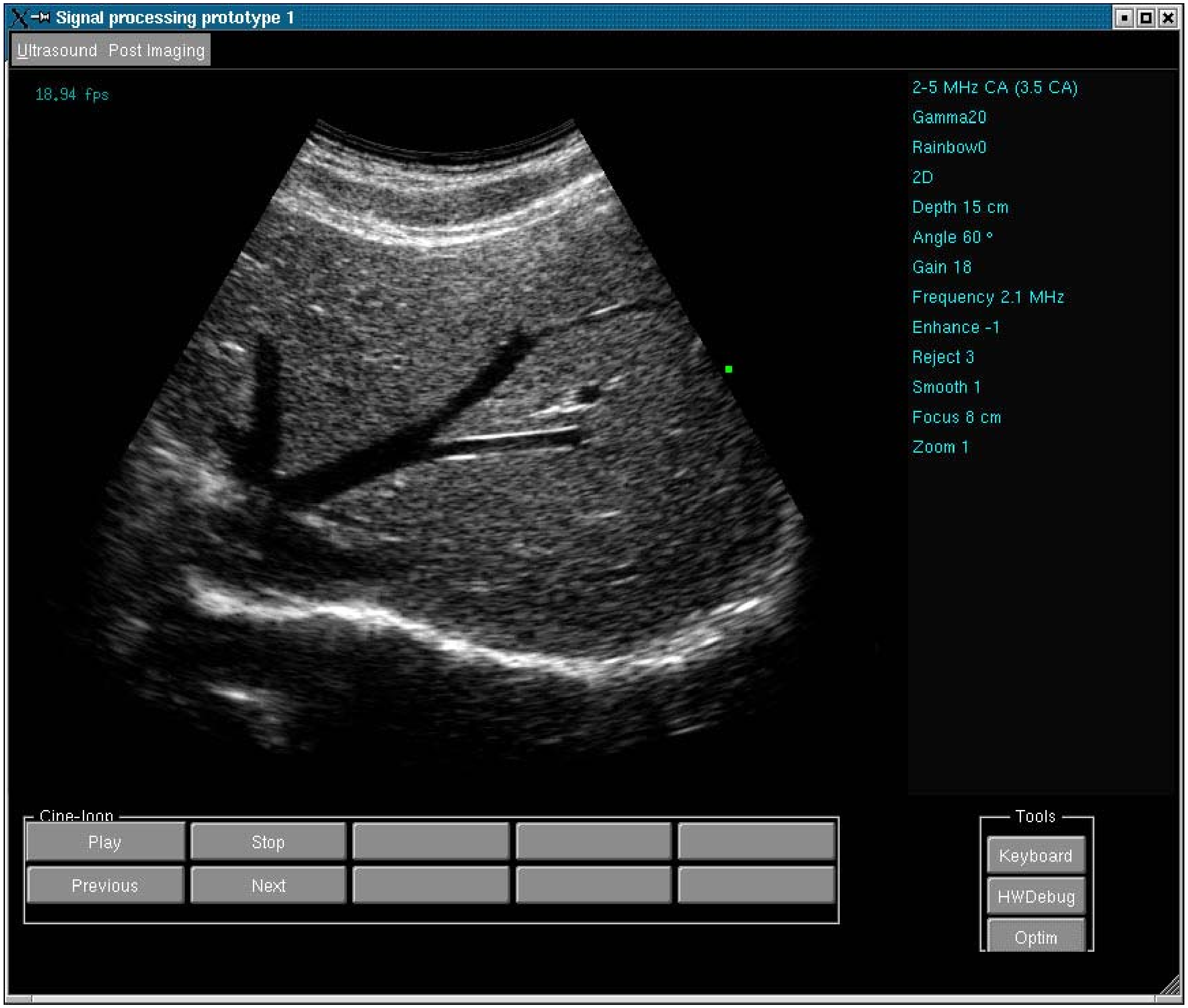
„First“ Images: Courtesy of Kontron Medical Inc.

Results: Heart



„First“ Images: Courtesy of Kontron Medical Inc.

Results: Liver



„First“ Images: Courtesy of Kontron Medical Inc.

Conclusion

- **A very flexible 64-channel digital beamformer for Medical Ultrasound imaging has been built from 9 FPGA‘s (Xilinx Virtex II).**
- **All signal processing takes place in the digital domain in the FPGA‘s. Remaining external frontend circuits are: Power amplifier for transmitter, preamplifier and A/D Converter for receiver.**
- **LVDS Double Data Rate links are a key element for mastering the large IO bandwidth required.**
- **The result is a compact and versatile high-performance imaging fontend for medical diagnostics.**

Thank you!

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